WISMO-CDMA

Q24X8 Product Technical Specification

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PRELIMINARY

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	Name	Function	Date	Signature
Written by	R Nixon	Dir. Of Hardware Dev.	2/17/2003	
Checked by				
Approved by				

Distribution List

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Overview

This document is intended to detail the Product Design of the Wavecom Q24x8 CDMA Module, allowing the customer to understand the function, capabilities and interface of the Module and integrate the Module into a viable consumer product.

1 Q24x8 Introduction

1.1 CDMA

Code Division Multiple Access, a cellular technology also known as **IS-95,** competes with GSM technology for dominance in the cellular world. There are now different variations, but the original CDMA is now known as **cdmaOne.** Developed originally by Qualcomm and enhanced by others, CDMA is characterized by high capacity and small cell radius, employing spread-spectrum technology and a special coding scheme. The Telecommunications Industry Association (TIA) adopted CDMA, in 1993. By December 2000, there were 80 million subscribers on cdmaOne systems worldwide.

In 1999 a new third generation (3G) standard was accepted, of which CDMA2000 is one of three operating modes (WCDMA and TD-SCDMA are the other two).

The Module provides peak data rates of up to 153 kbps, without sacrificing voice capacity for data capabilities. It allows for extended battery life and twice the system capacity over earlier products. The Module detailed in this document is based on this 1XRTT technology.

1.2 Safety and Governmental Agency Approval

The Q24x8 CDMA module shall comply with the following standards or guidelines:

- Formal Qualification Test, as mutually specified by Wavecom and manufacturer.
- IEC950, for electrical safety
- UL950, for electrical safety
- FCC Part 15B power supply, conducted requirements only
- FCC Part 22 (800 MHz), Part 24 (1900 MHz)
- SAR (host dependent)
- CSA for Canada
- Canada IC-133
- CDG 1, 2 (IS-98D, IS-898)
- CDG 3 (application specific)

2 General Description

Designed for fast and easy integration, this 2nd generation line of CDMA Modules includes the Q2438 Dual Band (800/1900 MHz) and the Q2458 Single Band (800 MHz) versions. The Modules provide handheld devices with wireless connectivity, high-speed reliable performance, and critical features such as gpsOne, AMPS and Open AT. The Q24x8 family is designed to target Wireless Local Loop, Telematics, Machine-to-Machine Interfaces, and Global Positioning Devices.

2.1 Product Features

- EVRC, 13kQCELP
- 153 kbps forward and reverse
- Circuit Switch (IS707-A.4)
- Packet Data (IS707-A.5)
- Class II G3 FAX
- gpsOne position location capabilities
- AMPS (Analog) voice
- RUIM (for China only)
- SMS (Mobile Originated and Mobile Terminated)
- OTASP, OTAPA
- IOTA
- Differential Audio: 60 pin Interface Connector
- TTY/TTD
- USB (population option)
- Wireless interface: CDMA2000 (IS-2000)
- BREW
- Open AT Platform
- Dimension: 58 x 32 x 3.9 mm (Including shielding)
- Weight: ~15 grams
- Operating Temperature: -30°C ~ +60°C
- Band (CDMA2000) – (Dual Band)
  - Band class 0 (TX: 824 ~ 849 MHz/ RX: 869 ~ 894 MHz)
  - Band class 1 (TX: 1850 ~ 1910 MHz/ RX: 1930 ~ 1990 MHz)

2.2 Radio Functionality

The radio design is based on the Qualcomm RadioOne direct conversion chipset. It supports the following four frequency bands and four operation modes.

- CDMA Band Class 0 (Cellular 800MHz Band)
- CDMA Band Class 1 (PCS 1900 MHz Band)
- AMPS (Cellular 800MHz Band)
- Qualcomm gpsOne (L1 1575.42MHz Band)

CDMA Cellular, CDMA PCS, and AMPS functions are supported through the same RF connection. The gpsOne has a separate RF connection. This allows the users to have more antenna selections and a more flexible design overall.

2.3 Baseband Functionality

The Q24x8 CDMA Module is based on the Qualcomm MSM6050 Mobile Station Modem.

The features of this solution include:

- Embedded QDSP2000 digital signal processor core, providing hardware support for features such as voice recognition, voice memo, speech compression, acoustic echo cancellation, audio automatic gain control (additional Software licensing is required)

- 4Mbytes of Flash (900kbytes available for customer applications)
- 2Mbytes of Pseudo SRAM (500kbytes available for customer applications)
- NAND Flash memory support
- Page mode NOR Flash/SRAM support
- CMX (text, picture and MIDI streaming: Software option– additional licensing required)
- Voice mode V1 (EVRC, 13k QCELP)
- ARM7TDMI embedded microprocessor subsystem
- Tri-Mode capable (CDMA cellular, CDMA PCS, AMPS cellular)
- General-Purpose Interface Bus
- Battery Management
- Charge Control
- Ringer driver
- RTC circuit
- USB support (population and Software option)
- Keypad (Software option)
- R-UIM

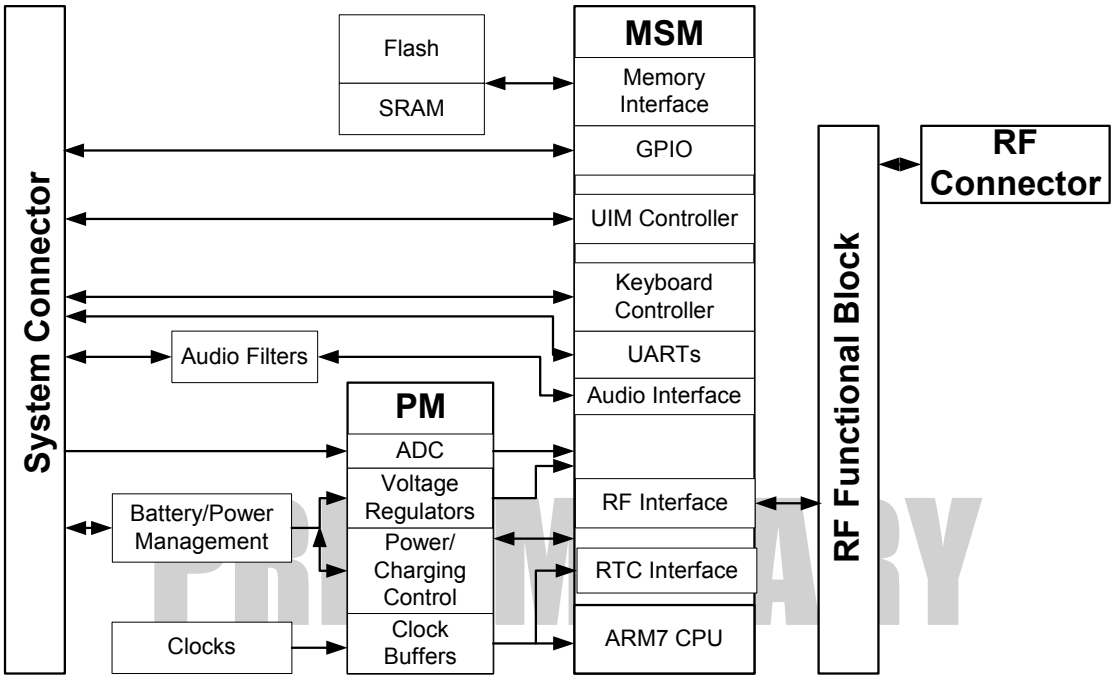
The Baseband is composed of three basic blocks; Power, Digital and System Connector.

The Power block is based primarily on the Qualcomm PM6000 Power Management IC. Within this chip are 7 controllable low dropout regulators; charging control lines and monitors; a 10-bit ADC with multiplexed inputs, and various clock buffers and current drivers. Control is via a 3 wire serial bus connected to the MSM.

The Digital block consists of the Qualcomm MSM6050 and one stacked memory part. The stacked memory includes both the SRAM and FLASH memory. The Flash within is a read-while-write part containing both the executable code and non-volatile parameters such as Calibration data. The Flash can be reprogrammed using the Wavecom Flash Download Tool running on a PC. This allows field upgrades of any embedded software.

The third block, the System Connector, is a 60-pin dual row surface mount component. The overall board-to-board stack height is 3.0 mm.

Figure 2-1 Q24x8 Block Diagram



2.4 Software Functionality

The Q24x8 CDMA Module embedded software supports the CDMA2000 Rev 0 Standard. In addition, features have been developed in the Module to support the various applications described in the following sections.

2.4.1 AT Commands

Extensive AT commands have been developed. They are the primary interface to the CDMA software, and they cover IS-707.5, applicable GSM AT commands, Qualcomm defined AT commands, Carrier specific AT commands, and Wavecom defined AT commands. For the detailed list of each AT command and its description, please refer to Wavecom *CDMA AT Commands Interface Specification*.

2.4.2 OPEN AT

OPEN AT provides a platform that allows Wavecom customers to develop an extended AT command set by themselves to address a greater range of control over the Module and to suit their needs. This increased flexibility and functionality allows customers to "tailor" Modules for their market by targeting their specific needs and requirements. Through OPEN AT SDK, customers are able to download their own AT commands and link with Wavecom CDMA software. For the detailed user guide of OPEN AT, please refer to *Wavecom OPEN AT User Guide*.

2.4.3 gpsOne

gpsOne technology merges Global Positioning System (GPS) satellite and network information to provide a high-availability solution that offers industry-leading accuracy and performance. This solution performs under the most challenging conditions and provides a platform for both location-based applications and FCC compliance. The Q24x8 provides multi modes of gpsOne operation as follows:

(1) Mobile-assisted Positioning (Smart Server): The mobile, using assistance information received from the network, makes pseudo range and pilot phase measurements and relays them to the PDE (Position Determination Entity). The PDE then calculates the mobile's position.

(2) Mobile-based Positioning (Thin Server): The mobile, using assistance information received from the PDE, makes pseudo range measurements and computes its own position.

2.4.4 R-UIM

The R-UIM (Removable User Identity Module) is required for China Market. The full functions of R-UIM including the R-UIM Tool Kit are supported.

2.4.5 IOTA

IOTA (IP-based Over-the-Air) provides a mechanism to automatically provision or retrieve configuration data from mobile terminals through any IP-based data connection. The use of IP provides maximum flexibility for application developers and customer support providers. Some carriers including Sprint now require this feature. The configuration data include NAM related parameters, Mobile IP profile, browser proxy address and home page, OEM info, firmware info, etc.

3 Hardware Interface

3.1 System Connector

A 60-pin connector is provided to interface the Module within the host application. The connector is a 0.5mm pitch surface mount board-to-board connector, equivalent to the Kyocera/AVX part number 14-5087-060-930-861. The mating part, required on the Host, is a Kyocera/AVX part number 24-5087-060-X00-861.

Unless otherwise noted, the typical interface voltage is referenced to the primary regulator for the digital processor, which is 2.8Vdc CMOS level.

See *System Connector* below for the individual pin assignments of the connector.

3.1.1 Power

Multiple pins on the System Connector are used to provide the input power to the Module.

These are referred to as +V_BAT. This input supplies the PM6000 chip and thus all regulators within the Module. In addition this input supplies the RF Power Amplifiers (via a FET switch that is used to isolate the battery from the Charger if required).

Although the PM chip can handle a broad range of input voltage, the RF amplifiers limit the acceptable range for the Module, as given below.

Table 3-1 Power Supply Voltage

	Vmin	Vnom	Vmax
+V_BAT	3.2Vdc	3.6Vdc	4.2Vdc

Ground for the Module is obtained through the shielding case of the Module itself. There is no connector pin provided for this. The shielding case has four pins (feet) that should be directly soldered through a ground layer on the host PCB to provide a suitable return path for the Module.

3.1.2 On-Off Control

There are two methods of turning the Module on. The primary method is via the ON/OFF pin on the System Connector. The alternative method is via the application of an external charger to the Module. Note that in the second case, the Module will come up in an Offline Mode, on and running however the RF deck is disabled.

3.1.2.1 ON/OFF Pin

Pin 6 of the System Connector is ON/OFF. This is configured to be both a logic level input, and a pulsed input. Refer to the following table for details.

Table 3-2 ON/OFF Pin Function

		ON	OFF
Pulse	Voltage (V)	2.0Vdc ≤ **V** ≤ +V_BAT+0.5Vdc (V ≤ 0.7Vdc when Low)	2.0Vdc ≤ **V** ≤ +V_BAT+0.5Vdc (V ≤ 0.7Vdc when Low)
	Time (T) *	**T** ≥ 0.1 Seconds	**T** ≥ 2.0 Seconds
Logic Level	Voltage (V)	2.0Vdc ≤ **V** ≤ +V_BAT+0.5Vdc	**V** ≤ 0.7Vdc
	Time (T) *	**T** ≥ 5.0 Seconds	**T** ≥ 2.0 Seconds

***Note**: The times **T** given in the table above are subject to change once more tests have been performed on prototype Modules. Also, the times **T** for the ON condition assume a valid supply voltage +V_BAT has already been applied.

The Pulse method is most appropriate when an external keypad is to be controlled by the Module. The Pulse method requires the external "on" key be connected to both this ON/OFF line and the keypad-scanning matrix.

3.1.2.2 External Charger On/Off

The application of an external charging supply to the CHG_IN (pins 1,2,4) will power on the Module in an Offline state (no RF capability). Refer to the *Charging* section for details on the charger itself and the requirements for this input.

3.1.3 Vcc_Out

The Module has a current limited regulated output voltage pin that can be used to supply some external circuitry on the host PCB. Pin 40 of the System Connector is Vcc_Out.

This line is sourced from the same regulator that is supplying the baseband processor and memory, and is thus only active when the Module in on. This regulator is enabled when the /Reset pin is initially pulled low, and has a settling time of approximately 1mS.

Table 3-3 VCC_Out Pin Specifications

Vcc_Out	Voltage (V)	2.887Vdc ±2%
	Current (I)	10mA maximum
	Temp Coeff	±100 ppm/°C

3.1.4 /Reset

Pin 14 of the System Connector is a bi-directional /Reset line. The internal reset for the Module is generated within the power management chip on the Module. This output then controls the processor and memories. It is this line that is also brought to the connector.

The host can use this signal to force a reset procedure to execute within the Module. This signal should be considered as an emergency reset only. If used, it has to be driven low by an external open collector or open drain source, as it is internally pulled up. The signal should be pulled low for a minimum of 20mS to guarantee a valid Module reset.

This signal can also be used to reset external circuitry if required. Again, it is active low and will stay low for 20 mS nominal.

3.1.5 Charging

The Q24x8 Module provides controlled charging of a Lithium Ion battery. A regulated external supply is required, to provide the constant current constant voltage source. This

should be connected to CHG_IN pins 1,2 and 4 of the System Connector. The application of the external charger will cause the Module to power up in an Offline Mode (no RF capability).

Internally the charging current will be gated to provide Trickle Charging, Constant Current charging, and finally Residual Charging.

> **Note:** The external supply must be a constant current constant voltage supply, with the current limit set to be the 1C rate of the battery (ex. A 1000mAh Li+ battery has a capacity C of 1000mAh thus the required 1C charge current is 1000mA), and the voltage limit set to be the recommended charge voltage for the particular cell being used. No regulation is provided within the Module.

3.1.5.1 Trickle Charging

Trickle charging is enabled automatically through software control when an external charger is applied and the main battery voltage is less than a set threshold. This is to prevent excessive current draw by the battery, minimizing heat and voltage fluctuations. The Module controls the appropriate trickle charging current and monitors the battery voltage to determine when to end trickle charging.

Table 3-4 Trickle Charge Specifications

	Typical	Units
Voltage Threshold	TBD	V
Current	TBD	mA

3.1.5.2 Constant Current Charging

When a Charger is applied to the Module and the main battery voltage is above the Trickle Charge Threshold, then Constant Current Charging will begin. The battery is charged at a current set by the external supply. As the battery voltage rises and approaches the desired value set by the constant voltage limiting of the external supply, the charging current begins to decrease. This marks the end of this cycle and the beginning of the Residual Charging.

3.1.5.3 Residual Charging

During charging of the main battery, the voltage of the battery will increase to a point where the voltage limiting of the external supply is reached. At this point the external supply current output will decrease exponentially, while the voltage remains constant at this set level. The Module will remain in this mode for TBD minutes to allow the Lithium Ion battery to become 100% charged. After this time, the battery will be isolated from the external supply to prevent over charging of the battery pack.

3.1.6 Digital I/O

There are 31 General Purpose Input/Outputs available on the Module. Many of these lines

have an alternate function selectable via Software. There are also differences in the pin characteristics so care must be taken in choosing a GPIO for the function desired.

Refer to the *System Connector* section for details on the pin numbers, the pin type (drive strength, pull up or pull down, etc), and the alternate function available.

3.1.7 LCD Interface

The Q24x8 does not provide a dedicated LCD interface. However GPIOs can be used to control an external serial LCD. The control lines and data lines would have to be individually manipulated, limiting the capability to a small monochrome display.

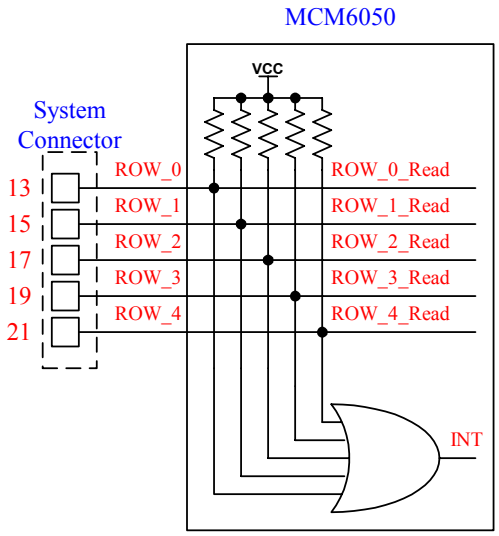
> **Note**: As every display is custom, this feature requires additional design effort and is not supported in the basic offering.

3.1.8 Keypad Interface

The Module provides optional support for a 5x5 keypad matrix. The ROW and COL lines of the System Connector, as given in the *System Connector* section, can be used to set up the scan matrix for the external keypad. The ROW pins have active pull-ups built in to reduce the need for external components, and are active-low level-sensitive inputs. The COL pins are provided by GPIOs configured to be outputs, toggled low by Software. When shorted to the ROW lines through the external matrix, an interrupt INT will be generated, the key press location decoded and reported. No external de-bouncing is required as this is provided for in Software.

> **Note**: The Keypad Interface is an alternate function provided by the embedded Software. The default configuration of these ROW lines and COL lines is as GPIO.

Figure 3-1 Keypad Interrupt Sense Circuit



3.1.9 Communication

The Q24x8 provides options on the number and type of serial communication interfaces with the host. Alternative embedded Software loads, and jumpers (resistors) populated during the production of the Module determine the availability and functionality of the interface pins of the Connector. A USB Interface, 2 UARTs, and various GPIO are configurable. Care must be taken in designing the appropriate interfaces, as not all are available simultaneously. *Figure 3-2*, *Table 3-5* and *Table 3-6* indicate the options available. Refer to the following sections for details.

Figure 3-2 Serial Communication Interface

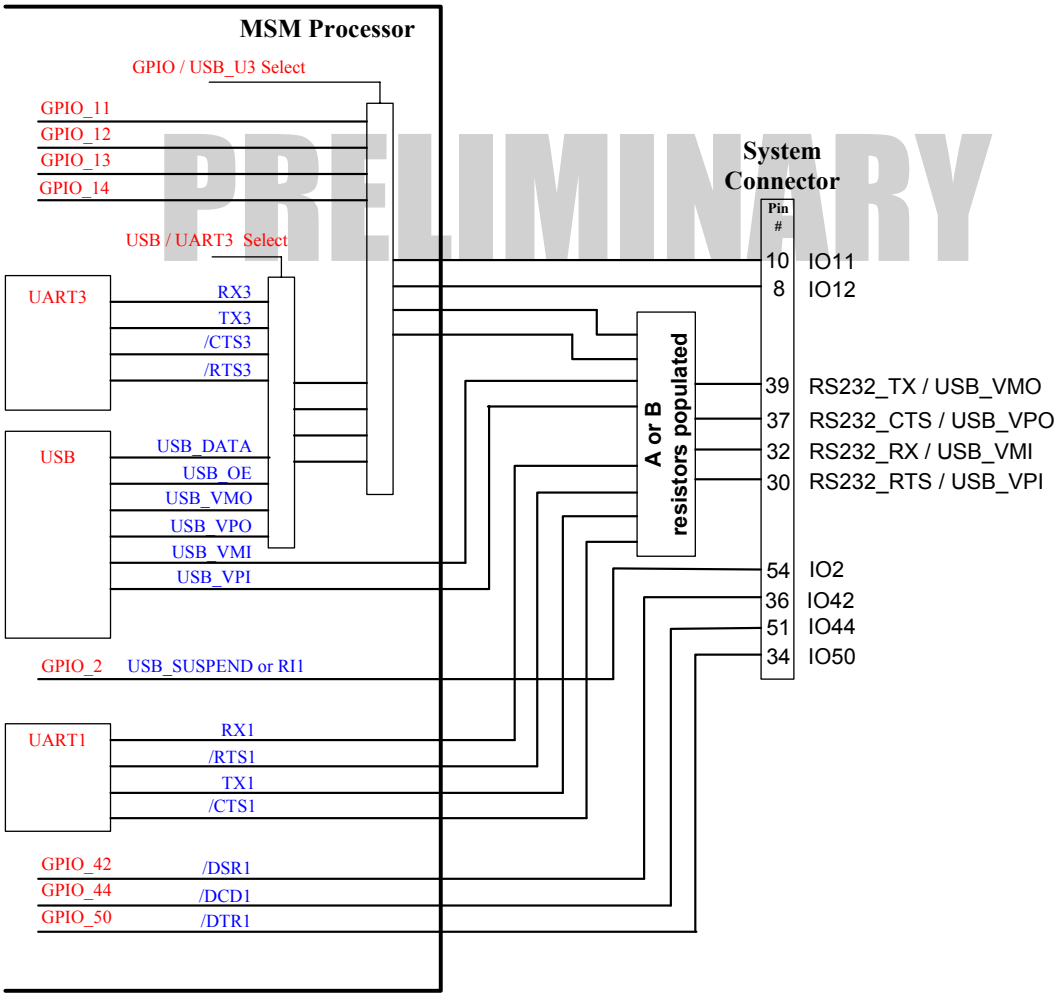


Table 3-5 Population Resistor A (Default configuration)

System Connector Pin Number	Default Function		Alternate Function 1		Alternate Function 2	
10	UART2 RX	I	GPIO 11			I/O
8	UART2 TX	O	GPIO 12			I/O
39	UART1 RX					I
37	UART1 CTS					O
32	UART1 TX					O
30	UART1 RTS					I
54	UART1 RI		O	GPIO 2		I/O
36	UART1 DSR		O	GPIO 42		I/O
51	UART1 DCD		O	GPIO 44		I/O
34	UART1 DTR		I	GPIO 50		I/O

Note: The default function of pins 8 and 10 may change to being the GPIOs, instead of the second UART, on future builds.

Table 3-6 Population Resistor Option B

System Connector Pin Number	Alternate Function 3		Alternate Function 4		Alternate Function 5	
10	USB_DATA			I	UART2 RX	I
8	USB_OE			O	UART2 TX	O
39	USB_VMO	O	USB_VMO	I/O	UART2 RTS	I
37	USB_VPO	O	USB_VPO	I/O	UART2 CTS	O
32	USB_VMI	I	GPIO 10			I/O
30	USB_VPI	I	GPIO 9			I/O
54	USB_SUSPEND			O	GPIO 2	I/O
36	GPIO 42					I/O
51	GPIO 44					I/O
34	GPIO 50					I/O

3.1.9.1 UART1

The Q24x8 contains a Universal Asynchronous Receiver Transmitter (UART) that communicates with serial data conforming to the RS-232 interface protocol. The UART1 can be used as a serial data port for data transfer, testing and debugging, and to load and/or upgrade the system software.

The UART1 uses 8 pins on the System Connector as shown in *Table 3-7*. The default population is with the UART1 Interface populated and enabled. This is Option "A", as shown in *Table 3-5* above, and in *Table 3-7* below.

Table 3-7 UART1 Pin Names and Numbers

Signal Name	I/O (wrt Module)		Description (wrt Host)	Sys. Conn. #
RS232-RX	O	Module -> Host	Receive serial data	32(A)
RS232-TX	I	Host -> Module	Transmit serial data	39(A)
RS232-RTS	I	Host -> Module	Request To Send	30(A)
RS232-CTS	O	Module -> Host	Clear To Send	37(A)
IO44 (DCD)	O	Module -> Host	Data Carrier Detect	51
IO2 (RI)	O	Module -> Host	Ring Indicator	54
IO50 (DTR)	I	Host -> Module	Data Terminal Ready	34
IO42 (DSR)	O	Module -> Host	Data Set Ready	36

*(A) indicates that resistor networks were populated to enable the "A" option of UART.

*wrt = "with respect to"

3.1.9.2 UART2

The Module supports an optional second UART, UART2 (connected internal to the Module to UART-3 of the MSM processor, as shown in the block diagram above). The UART2 is either a two-wire interface (RX2 and TX2), or a four-wire interface (with additional RTS2_N and CTS2_N). However because of some shared functionality on the connector pins, use of the four-wire interface precludes the use of both the USB and UART1, as shown above.

3.1.9.3 USB

The Q24x8 is capable of supporting a Universal Serial Bus (USB). The Modules USB interface is USB Rev 1.1 compliant, and USB Rev 2.0 compliant (12Mbps only) however an external USB transceiver is required to implement the interface. There are 7 lines required to support the USB.

The USB interface supports connections to transceivers with both separate input and output data pins (Philips ISP1106) or with bi-directional data pins (Micrel MIC2550). The embedded Software is used to determine which style of USB interface is preferred, however Module Hardware must be populated to enable the USB control lines. This is

Option “B”, as shown in *Table 3-5* above, and in Table 3-8 below.

Table 3-8 USB/UART-2 Pins and Connections

Signal Name	Philips ISP1106	Micrel MIC2550	System Conn. #
USB-VMI	VM	Not used	32(B)
USB_VMO	VMO	VM	39(B)
USB_VPI	VP	Not used	30(B)
USB-VPO	VPO	VP	37(B)
USB_OE	OE/	OE/	8
USB_DATA	RCV	RCV	10
USB_SUSPND	SUSPEND	SUS	54

*(B) indicates that resistor networks were populated to enable the “B” option of USB.

The following figures show the connections between the System Connector and the two external transceivers, one of which the user must use if USB is desired. Refer to the appropriate data sheet for each transceiver connection requirements.

Figure 3-3 Example Connections for Philips ISP1106 Transceiver

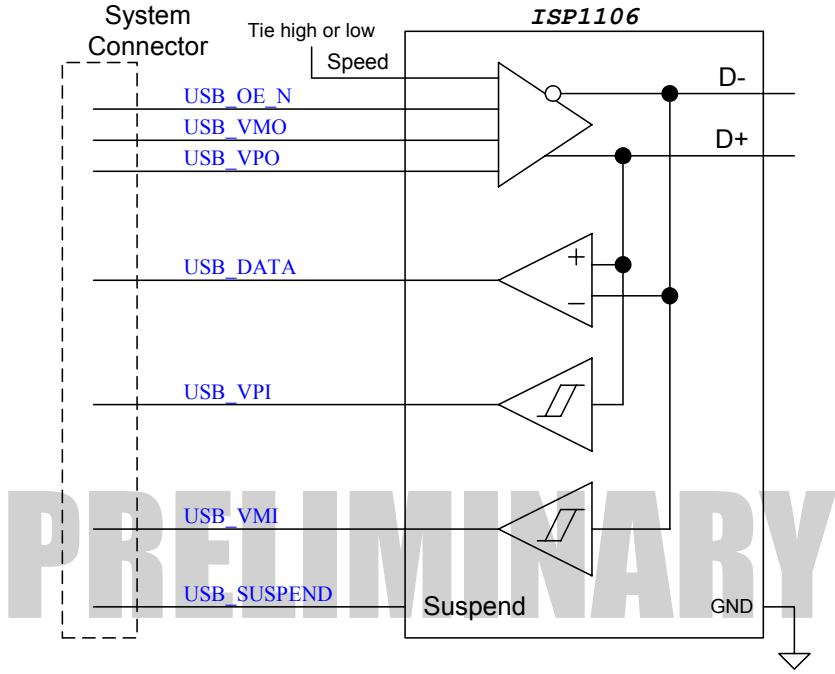
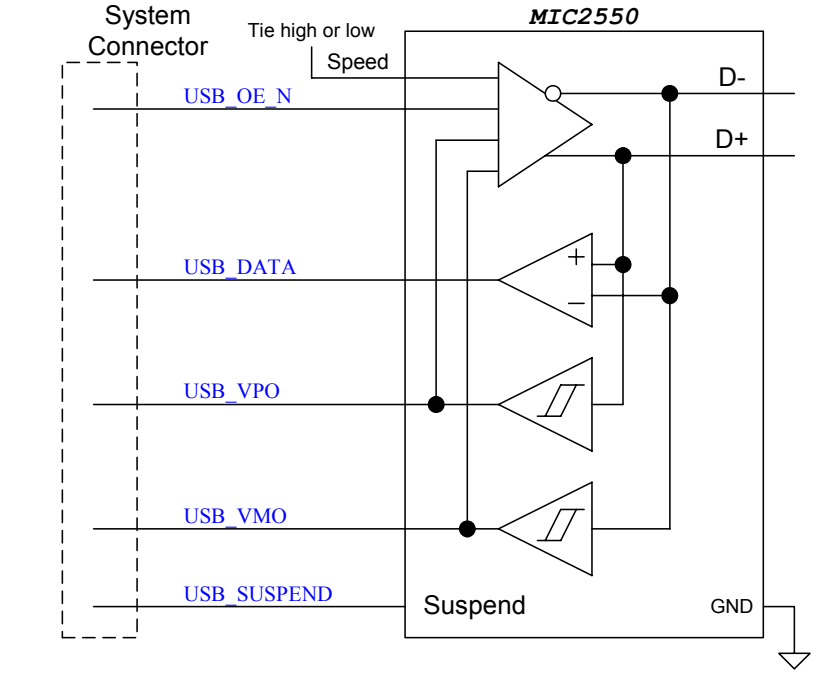


Figure 3-4 Example Connections for Micrel MIC2550 Transceiver



3.1.10 R-UIM Interface

The Removable User Identity Module (R-UIM) is a smart card for CDMA cellular applications. The Q2458 (Single Band Module) can support a 3.0 Volt R-UIM interface, as required in the China marketplace.

Two of the 4 required lines, R-UIM_CLK pin 3 of the System Connector and R-UIM_Data pin 7, are dedicated pins on the interface. The other two lines, R-UIM_RST and R-UIM_PWR_EN, are GPIO lines under Software control.

Table 3-9 R-UIM Pin Functionality

Pin Number	Signal Name	Alternate Function
3	R-UIM_CLK	
5	GPIO_INT_49	R-UIM_RST
7	R-UIM_Data	
9	GPIO_INT_56	R-UIM_PWR_EN

Note: Pins 5 and 9 are available as standard GPIO if the R-UIM is not required.

The R-UIM_PWR_EN line is used to enable an LDO regulator in order to supply power to the R-UIM. The R-UIM has a maximum constant current draw of 50 mA and can spike to 50 mA above this level. Refer to the R-UIM specification for further details.

3.1.11 Analog to Digital Converter

The System Connector has 2 general-purpose Analog-to-Digital Converter inputs, ADC_0 and ADC_1 on pins 33 and 38 respectively. The two inputs, along with internal inputs, are multiplexed into one converter within the Module. The user can determine the functionality of these two external channels.

Table 3-10 ADC Analog Input Specification

Parameter	Conditions	Min.	Typ.	Max.	Units
Channel Isolation	f = 1KHz		50		dB
Resolution			10		bits
Input voltage range		0		2.5	V
Input impedance: Resistance Capacitance	Parallel RC	 3		 10	 MΩ pF
Input Bandwidth	0Ω source impedance		TBD		KHz
Full scale error				±3	%
Offset error				5	LSB

Sampling clock freq.	From internal RC oscillator	0.96	1.28	1.92	MHz
Conversion timing				43	µsec

3.1.12 Audio Interface

The Q24x8 provides audio input and output on the System Connector. The System Connector provides for two microphones and two speakers to be connected, with either pair being selectable via AT Commands.

3.1.12.1 Microphone

The System Connector provides two microphone interfaces to the main board. Both the primary interface (MIC_1) and secondary (MIC_2) are differential interfaces. Either can of course be used in a single-ended application (such as for a headset) however the differential configuration is recommended to help reduce noise.

Figure 3-10 is example of a differential microphone in a typical handset application.

Figure 3-5 MIC_1 Differential Interface

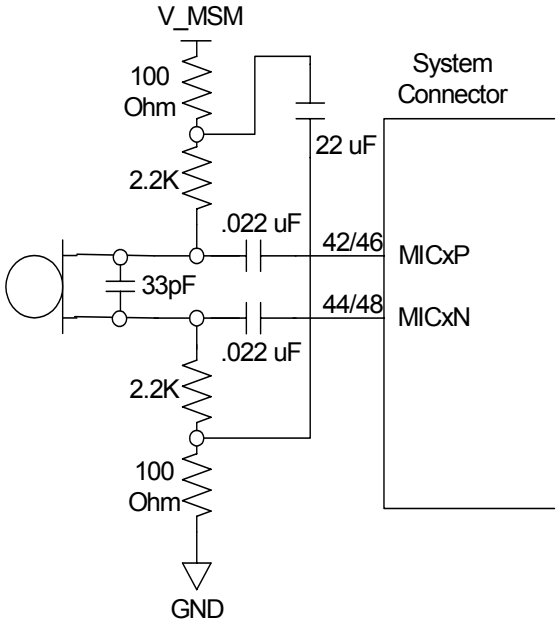
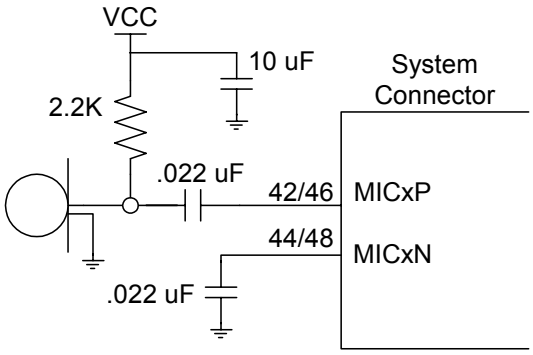


Figure 3-11 is example of a single-ended microphone in a typical handset application.

Figure 3-6 MIC_2 Single-Ended Interface



3.1.12.2 Speaker

The System Connector provides two speaker interfaces to the main board. The primary interface (SPK_1) is a differential interface. This interface is the preferred receive path as the differential circuitry will help to minimize noise at the speaker. The secondary interface (SPK_2) is single-ended. The single-ended application is normally used for the headset, which by nature typically requires a single ended driver.

Figure 3-12 is example of a differential speaker in a typical handset application.

Figure 3-7 SPK_1 Differential Interface

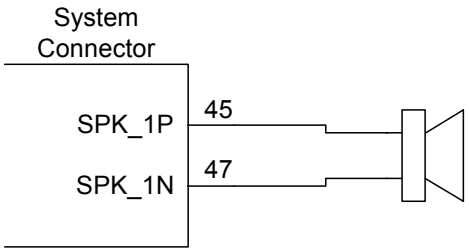


Figure 3-13 is example of a single-ended speaker in a typical handset application.

Figure 3-8 SPK_2 Single-Ended Interface

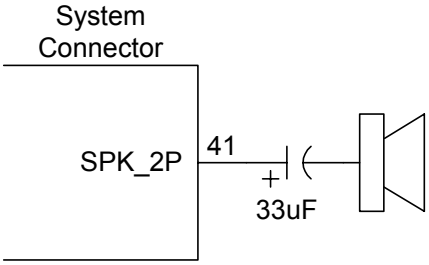


Table 3-11 Speaker Amplifier Power

	Max output power, +3 dBm0 sine wave into 32 Ohm speaker
SPK_1 (differential)	35mW
SPK_2 (single-ended)	8.8mW

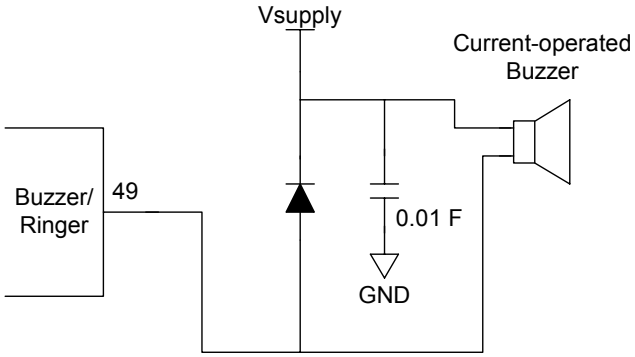
3.1.12.3 Ringer

The Q24x8 Module provides a Ringer or buzzer driver (sink) via pin 49 of the System Connector. A pulsed digital waveform is generated within the MSM via AT Commands that control the pitch (programmed frequency) and loudness (programmed duty cycle). The pulse stream can be a single tone or the sum of two different frequencies or DTMF tones. This waveform becomes the input single to a driver contained within the PM chip. The driver is a current sink, so the external ringer or buzzer device must be externally connected to a current source, with the Module providing the return-to-ground path for the device. A fly-back diode and decoupling capacitor are recommended to prevent voltage spikes that might damage the Module, and to minimize switching noise of the device.

Table 3-12 Ringer Driver Specifications

	Min	Typ	Max	Units
Load current	300			mA
Load resistance	7	10		Ω

Figure 3-9 Ringer: External Circuit example



3.2 RF Connection

The RF connections are 50-ohm impedance systems and are a DC short to ground. Best effort should be made to provide low insertion loss and shielding between the external antenna and RF connections over the frequency band interested. Also, keep the external RF cable away from any possible interference sources; especially high-speed digital signals and switching power supply.

The gpsOne receiver is very sensitive to interference and noise. Some isolation is required between these two RF connections even though gpsOne uses a different frequency than Cellular and PCS. Typically a minimum of 15dB isolation between these two signals should be maintained. If long cables are necessary for both RF connections, avoid putting these two cables side-by-side for long distances.

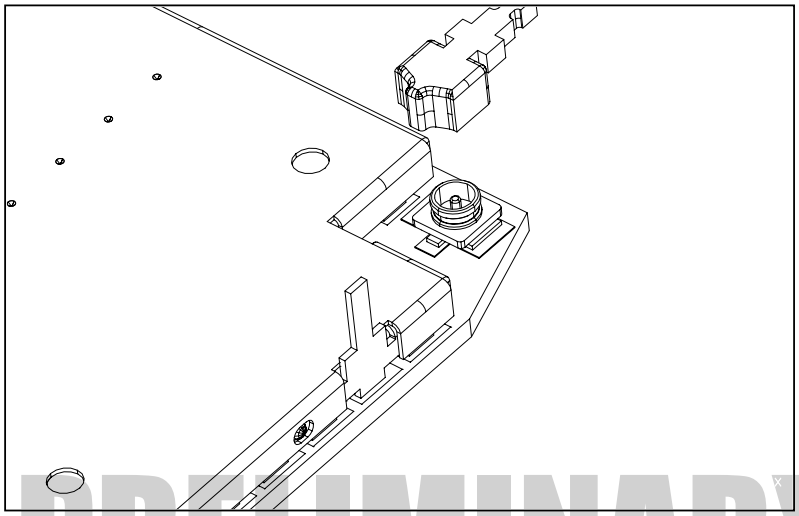
3.2.1 Cellular and PCS

There are three options available to connect the Module to an external antenna.

3.2.1.1 Option 1

A Hirose U.FL connector is available on the Module upon the request of the user. The connector is located on the component side of the Module as shown in Figure 3-10. The total mating height is 2.5mm. A right-angle plug shell with cable harness is available from Hirose. Please contact Hirose for detail specifications.

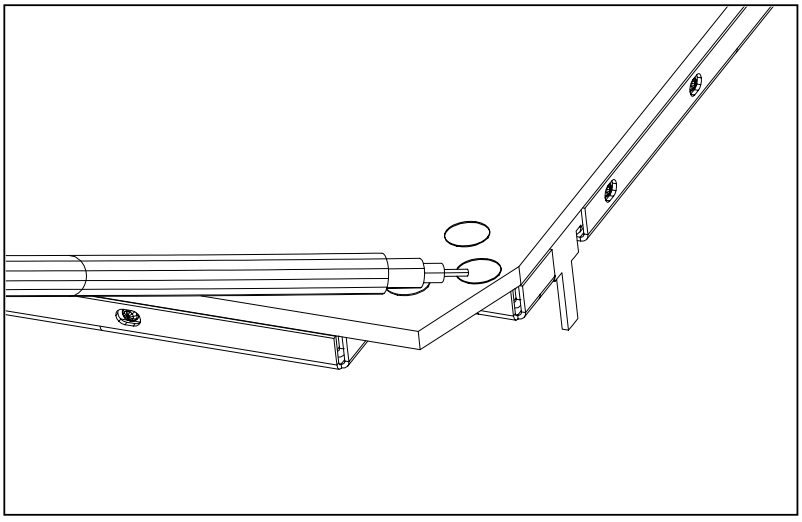
Figure 3-10 Ringer: RF Connection Option One



3.2.1.2 Option 2

A RG178 pigtail cable can be soldered to the component side as shown in Figure 3-11. Proper soldering of the cables ground shielding to the solid ground pad of the Module is essential for good RF performance. Adequate solder must be applied at the solder points to ensure a solid mechanical mount of the cable, preventing the possibility of the cable assembly breaking loose and shearing off the signal pad. Avoid putting excessive solder to reduce the parasitic capacitance on this line.

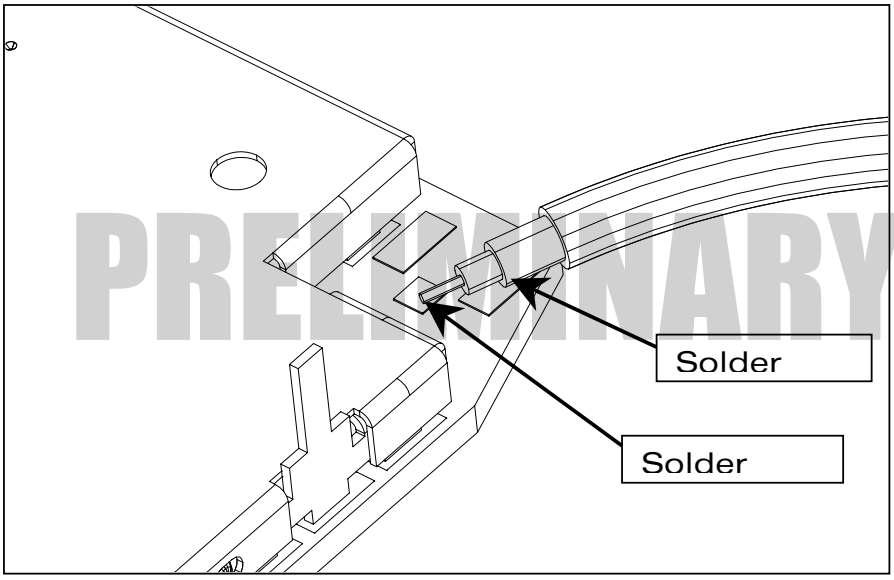
Figure 3-11 Ringer: RF Connection Option Two



3.2.1.3 Option 3

A RG178 pigtail cable can be soldered to the non-component side of the Module, as shown in Figure 3-12. Again, proper ground soldering of the cable is essential.

Figure 3-12 Ringer: RF Connection Option Three



3.2.2 gpsOne

Only the pigtail cable connection is available for gpsOne applications. The loss between antenna and this connection should be minimized to guarantee the performance of the gpsOne function. The soldering pads are very similar to the RF connection option three.

3.2.3 Antenna

The following details the recommended antenna requirements.

Table 3-13 Antenna Requirement

	Cellular	PCS	gpsOne
Freq. Range	824 – 894 MHz	1850 – 1990 MHz	1574 – 1576 Mhz
Impedance	50 ohm		
VSWR	1.5:1 max		

Gain	0 dBi in one direction at least

Note: Depending on applications, the requirement of the gain will be different. Typically, the higher the antenna gain, the more directional the antenna is.

4 Software Interface

The external applications communicate with Q24x8 Module through AT commands as specified in the *WismoQuick AT Interface Specification*.

5 CDMA – GSM/GPRS Design Differences

Although the pin outs for both the CDMA Module with the GSM/GPRS Module designs are identical, and every attempt has been made to ensure the complete compatibility of the designs, there are some particular areas where care must be taken to allow a "plug and play" swap of the two Module families.

5.1 Power Supply

The maximum voltage of the CDMA Module is 4.2Vdc. The GSM Module maximum is 4.5Vdc.

5.2 BOOT

To allow the customer to download new firmware into the Module, the GSM design requires the use of the BOOT line. The CDMA design does not require this line. This line on the CDMA Module is treated as a GPIO.

5.3 Audio

The CDMA Module provides only a single ended driver for the second speaker audio path. The GSM family has a differential driver here. Although any external circuit design making use of the differential drive will be compatible with the CDMA Module, the CDMA Module will have a relatively reduced drive level (6dB) on this audio speaker path compared to the GSM.

5.4 SIM / R-UIM

The GSM SIM card spec requires a maximum of 10mA supply to the card. However the R-UIM specification from Qualcomm specifies a higher current requirement for this supply. Care must be taken to ensure that adequate current is available to the R-UIM card. Refer to the *R-UIM Interface* section above for the requirements and recommendations.

6 Technical Specification

6.1 System Connector

Table 6-1 I/O Pin Parameters

Symbol	Description
Type	
B	Bi-directional
BS	Bi-directional with Schmitt trigger
CCS	Controlled Current Sink
CHV	Input Charging Voltage
I	CMOS input
IS	Input with Schmitt trigger
O	Output
V	Power
Special Circuitry	
A	Analog pad
PU	Contains internal pull-up device
PD	Contains internal pull-down device
KP	Contains an internal weak keeper device. Keepers cannot drive external busses
H	Digital input where input voltage level may reach up to 3.6 V
(1,2,5, etc.)	Values are the +/- maximum current drive strength in mA for output pins
n[m]	Variable drive strength pins. The number 'n' is the drive strength when the PAD_CTL register bit is clear (0). The Number [m] is the drive strength when the PAD_CTL bit is set (1).

Table 6-2 Interface Connector Pin Assignment

Pin #	Signal Name	Pin Type	Alt Function	Alt Function
1	CHG_IN			

2	CHG_IN			
3	R-UIM_CLK	BS-PD3[5]		
4	CHG_IN			
5	GPIO_INT_49	BS-PD3[5]	R-UIM_RST	
6	ON_/OFF	0 - VBATT		
7	R-UIM_Data	BS-PD3[5]		
8	GPIO_INT_12	BS-PD3[5]	TX2	USB-OE
9	GPIO_INT_56	BS-PD3[5]	R-UIM_PWR_EN	
10	GPIO_INT_11	BS-HK2	RX2	USB-DATA
11	No Connect			
12	GPIO_INT_6	BS-PD3[5]		
13	GPIO_INT_62	BS-PU3[5]	ROW_0	
14	/RST_IO	0 – 2.8v		
15	GPIO_INT_63	BS-PU3[5]	ROW_1	
16	GPIO_INT_3	BS-PU3[5]		
17	GPIO_INT_64	BS-PU3[5]	ROW_2	
18	GPIO_INT_4	BS-PD3[5]		
19	GPIO_INT_65	BS-PU3[5]	ROW_3	
20	GPIO_INT_15	BS-PU3[5]		
21	GPIO_INT_66	BS-PU3[5]	ROW_4	
22	GPIO_INT_16	BS-PU3[5]		
23	GPIO_INT_61	BS-PD3[5]	COL_0	
24	GPIO_INT_17	BS-PU3[5]		
25	GPIO_INT_60	BS-PD3[5]	COL_1	
26	GPIO_INT_18	BS-PD3[5]		
27	GPIO_INT_59	BS-PD3[5]	COL_2	
28	GPIO_INT_19	BS-PD3[5]		
29	GPIO_INT_58	BS-PD3[5]	COL_3	
30-A	RS232-RTS	IS-PU		
30-B	USB_VPI	BS-HK2	GPIO 9	
31	GPIO_INT_57	BS-PD3[5]	COL_4	
32-A	RS232-RX	O-3[5]		

32-B	USB_VMI	BS-HK2	GPIO 10	
33	ADC_0	IA		
34	GPIO_INT_50	BS-PU3[5]	DTR	
35	GPIO_INT_48	BS-PU3[5]		
36	GPIO_INT_42	BS-PD3[5]	DSR	
37-A	RS232-CTS	O-3[5]		
37-B	USB_VPO	BS-PD3[5]	UART2 CTS	
38	ADC_1	IA		
39-A	RS232-TX	IS-PD		
39-B	USB_VMO	BS-PD3[5]	UART2 RTS	
40	VCC-Out_2.8v			
41	SPK_2P	OA		
42	MIC_2P	IA		
43	GND			
44	MIC_2N	IA		
45	SPK_1P	OA		
46	MIC_1P	IA		
47	SPK_1N	OA		
48	MIC_1N	IA		
49	BUZ	?		
50	GPIO_INT_37	BS-PU3[5]		
51	GPIO_INT_44	BS-PU3[5]	UART1 DCD	
52	GPIO_INT_41	BS-PD3[5]		
53	GPIO_INT_54	BS-PD3[5]		
54	GPIO_INT_2	BS-PU3[5]	UART1 RI	USB-SUSPND
55	+Vbatt			
56	GPIO_INT_5	BS-PD3[5]		
57	+Vbatt			
58	+Vbatt			
59	+Vbatt			
60	+Vbatt			

6.2 DC Electrical Specifications

6.2.1 Absolute Maximum Ratings

Operating the Q24x8 under conditions that exceed those listed in Table 6-3 may result in damage to the device. Absolute maximum ratings are limiting values, and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the WISMOCDMA under any other conditions in Table 6-3 is not implied.

Table 6-3 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage temperature	TS	-55	+150	C
Supply voltage (Battery)	VBATT	-0.5	4.2	Vdc
Supply voltage (Charger)	CHG_IN	-0.5	4.2	Vdc
Voltage applied to any input or output pin	Vin	-0.5	VCC + 0.5	Vdc

6.2.2 Recommended Operating Conditions

Table 6-4 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambiant operating temperature	TS	-30	-	+60	C
Battery supply voltage	VBATT	3.2	3.6	4.2	Vdc
Charger supply voltage	CHG_IN	4.2	4.2	4.2	Vdc

6.2.3 DC Characteristics

Table 6-5 DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
High-level input voltage, CMOS/Schmitt	V_IH	0.65xVccP	-	VccP+0.3	Volts
Low-level input voltage, CMOS/Schmitt	V_IL	-0.3	-	0.35xVccP	Volts
Input high leakage current	I_IH	-	-	2	uA
Input low leakage current	I_IL	-2	-	-	uA
Input high leakage current with pull-down	I_IHPD	10	-	60	uA
Input low leakage current with pull-up	I_ILPU	-60	-	-10	uA
High-level, three-state leakage current	I_OZH	-	-	2	uA
Low-level, three-state leakage current	I_OZL	-2	-	-	uA
High-level, three-state leakage current with pull-down	I_OZHPD	10	-	60	uA
Low-level, three-state leakage current with pull-up	I_OZLPU	-60	-	-10	uA
High-level, three-state leakage current with keeper	I_OZHKP	-25	-	-3	uA
Low-level, three-state leakage current with keeper	I_OZLKP	3	-	25	uA
High-level output voltage, CMOS	V_OH	VccP-0.45	-	VccP	Volts
Low-level output voltage, CMOS	V_OL	0.0	-	0.45	Volts
Input capacitance	C_IN	-	-	15	pF
ADC Full-Scale Input Range	A_FS	GND	-	V_RT	-
ADC Input Serial Resistance	A_ISR	-	5	-	Kohm
ADC Input capacitance	A_C_IN	-	12	-	pF
Input offset voltage at MIC1, MIC2	MV_IO	-5	-	+5	mV
Input bias current at MIC1, MIC2	MI_IB	-200	-	+200	nA
Input capacitance at MIC1, MIC2	M_CI	-	5	-	pF
Input DC Common Mode Voltage	-	0.85	0.9	0.95	V
Microphone Bias supply voltage	MBIAS	1.69	1.8	1.91	V
MBIAS Output DC source current	-	1	1.07	-	mA
Input impedance MIC1, MIC2	M_ZIN	62	72	82	Kohm

6.3 RF System Specification

The RF performance is compliant with IS-98D or 3GPP2 Mobile Station Minimum Performance Specification for CDMA operation in Cellular band and PCS band. The AMPS performance is compliant with IS_98B analog mode or IS-19C. Please refer to those documents for detailed specifications and test methods. The maximum transmit power and receiver sensitivity at different modes are listed below in Table 6-6.

Table 6-6 RF Power/Sensitivity

Band	Spec	Min	Nominal	Max
Cellular	Max Output Power	23 dBm	24 dBm	30 dBm
		(200 mW)	(250 mW)	(1 W)
	Sensitivity		-107 dBm	-104 dBm
PCS	Max Output Power	23 dBm	24 dBm	30 dBm
		(200 mW)	(250 mW)	(1 W)
	Sensitivity		-106 dBm	-104 dBm
AMPS	Max Output Power	22 dBm	28 dBm	30 dBm
		(160 mW)	(630 mW)	(1W)
	Sensitivity		-118 dBm	-116 dBm

6.4 Power Consumption

Table 6-7 Power Consumption

Operating Mode	Band	Average	Units	Notes
CDMA RxTx Full Power	Cellular	TBD	mA	
	PCS	TBD		
CDMA RxTx Average Power	Cellular	TBD	mA	
	PCS	TBD		
CDMA Rx Active	Cellular	TBD	mA	
	PCS	TBD		
CDMA Sleep	Cellular	TBD	mA	
	PCS	TBD		

7 Mechanical

Figure 7-1 Module Mechanical Drawing